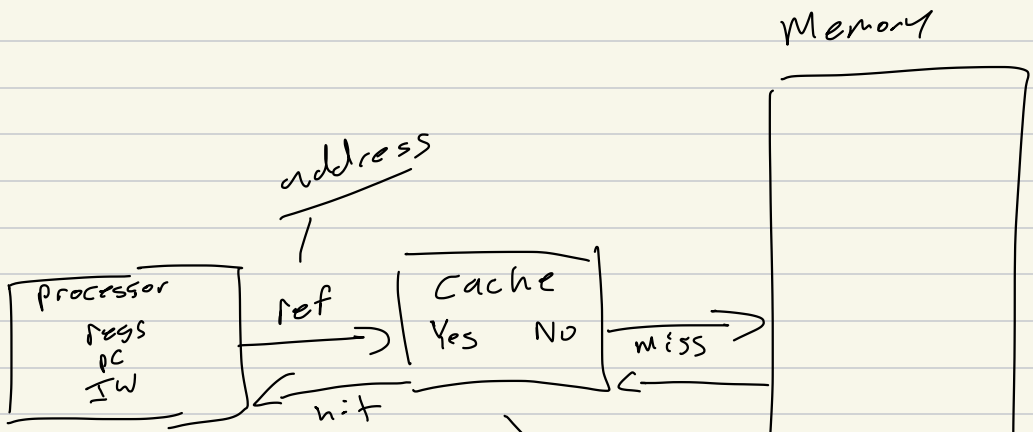
CS631-01 Cache Memory 2026-03-31

Project01 due Thu Apr 2 11:59 pm

1) RISC-V Emulation
2) Dynamic Analysis
3) Cache Simulation



refs

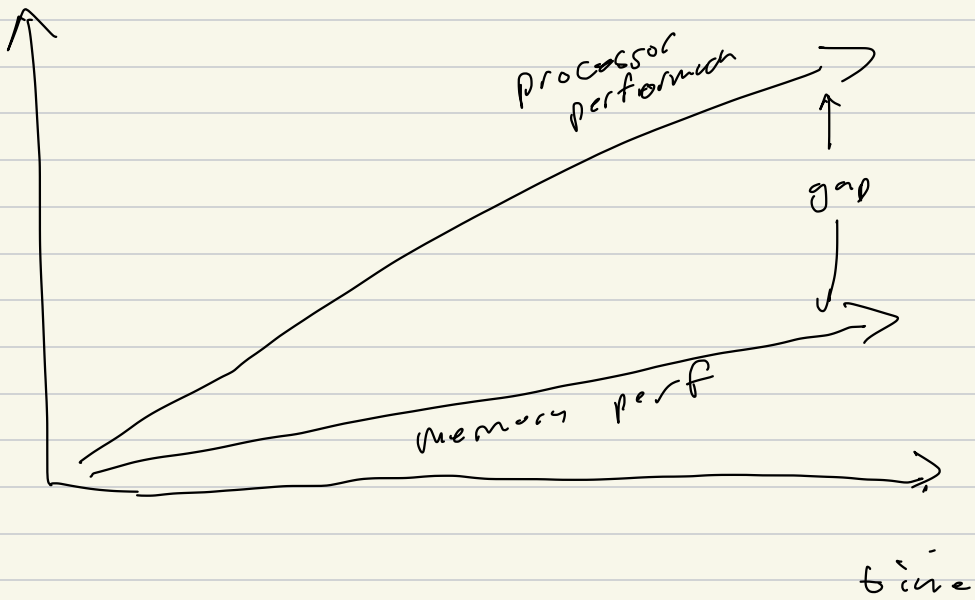
hits

misses

$$\text{hit rate} = \frac{\#\text{ hits}}{\#\text{ refs}}$$

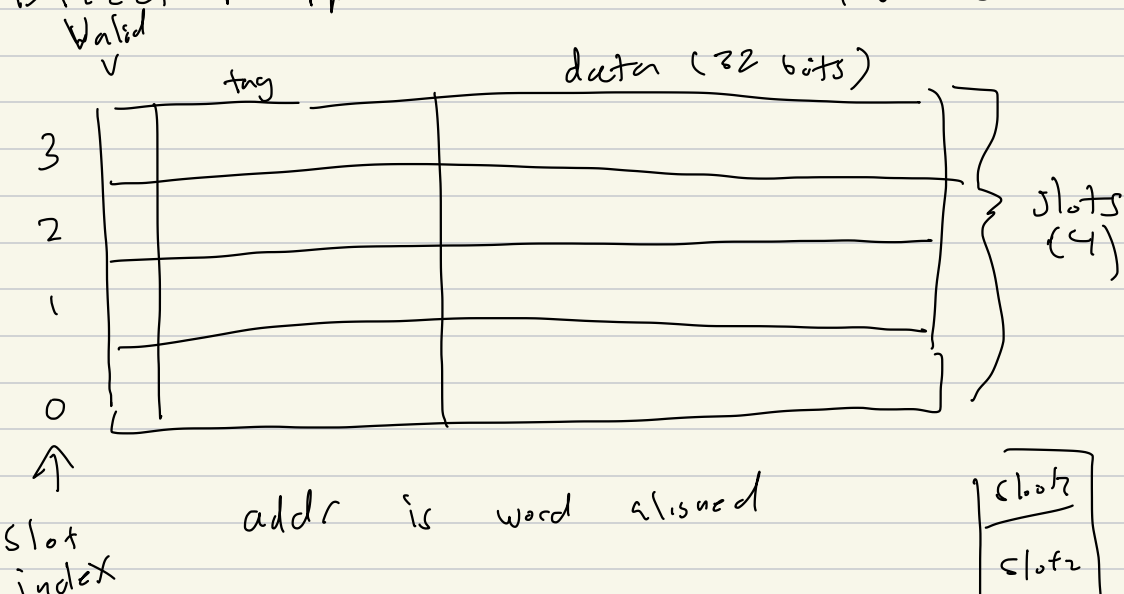
Questions:

1) Where to look for a given addr?
2) How to know if data is in cache?
3) How to resolve a conflict?


processor performance
gap
memory perf
time

Direct Mapped Cache

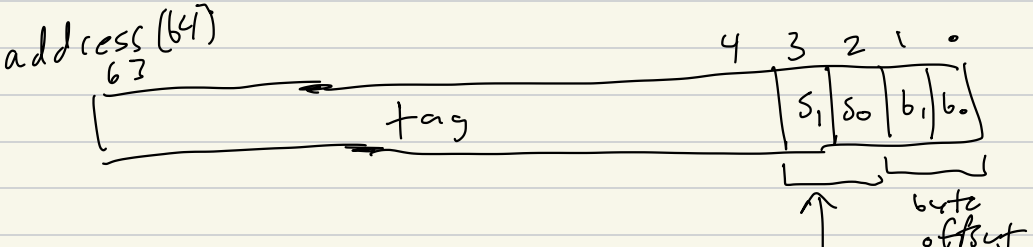
4 word cache



addr is word aligned

$addr\_word = addr_{byte} / 4$

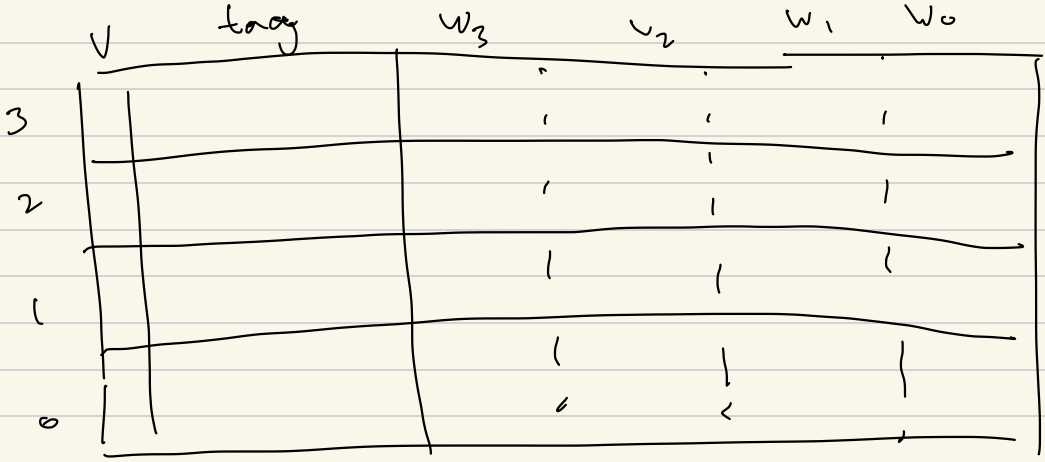
$slot\_index = addr\_word \ \%\ 4$



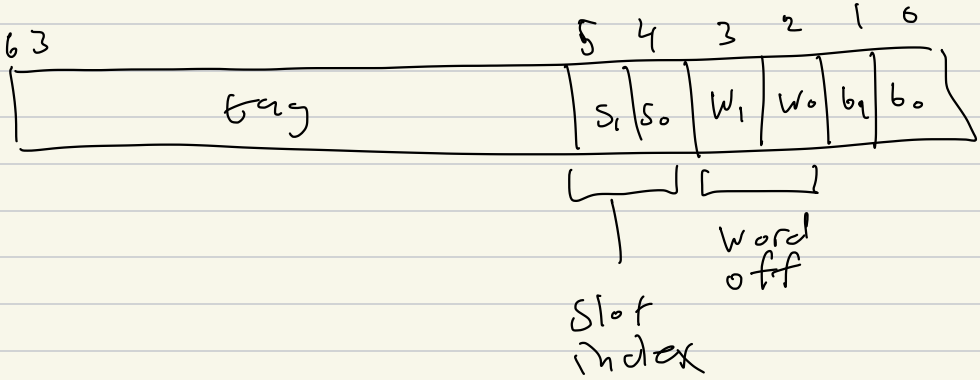
$slot\_index = (addr >> 2)\ \&\ 0b11$

$tag = addr >> 4$

Block size



addr



Set Associative Cache